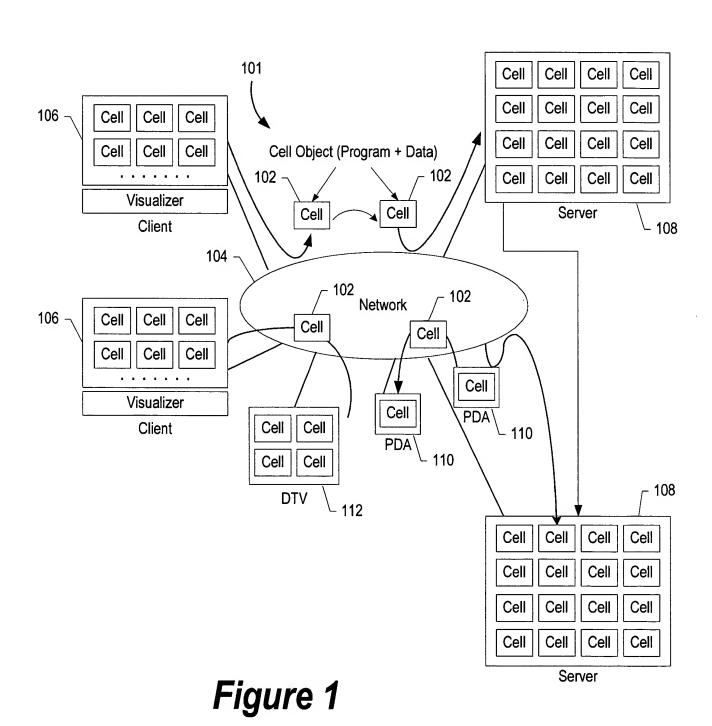EL977166465US

Fil : 3050.VSD   Docket No. AUS920030791US1
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Figure 1

Processor Element (PE)

<u>201</u>

PE Bus

<u>223</u>

PU
<u>203</u>

DMAC
<u>205</u>

<u>227</u>

DRAM
<u>225</u>

SPU
<u>207</u>

SPU
<u>209</u>

SPU
<u>211</u>

SPU
<u>213</u>

SPU
<u>215</u>

SPU
<u>217</u>

SPU
<u>219</u>

SPU
<u>221</u>

Figure 2

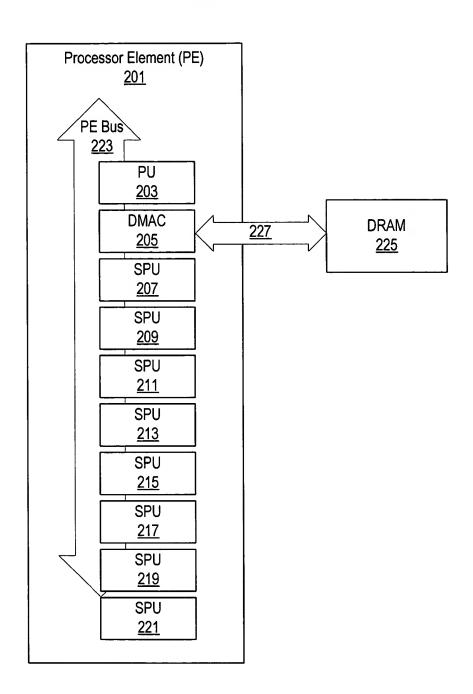File: 3050.VSD   Docket No. AUS920030791US1
Aguilar, et al.
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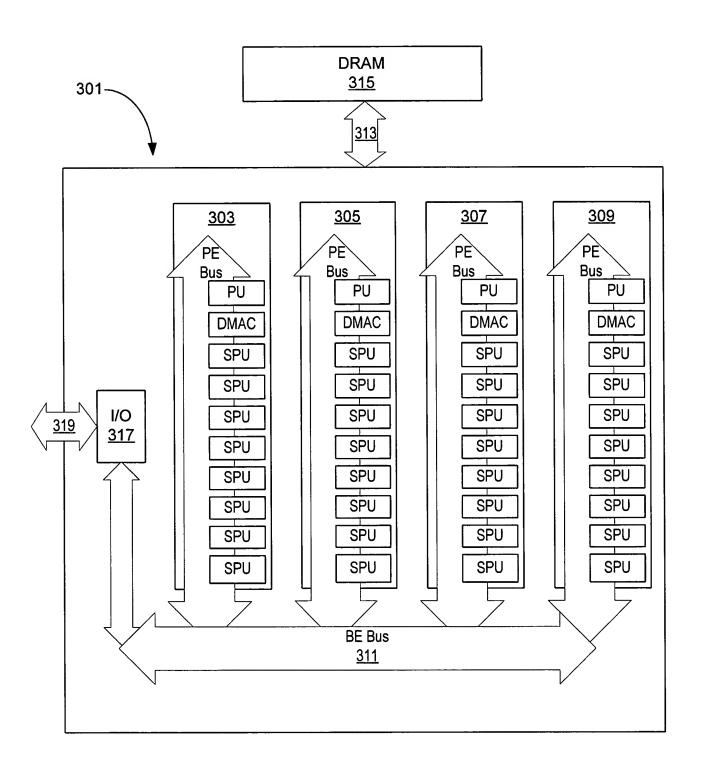**Figure 3**

Fil : 3050.VSD   D cket N . AUS920030791US1
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Figure 4

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                        Aguilar, t al.
  Syst m and Meth d f r Proc ss r Dedicated C de Handling in a Multi-Pr cessor Environment

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Figure 5

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                        Aguilar,   t al.
      Syst m and M thod f r Pr c ssor Dedicated Cod Handling in a Multi-Pr cessor Envir nment

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Figure 6

File: 3050.VSD   Docket No. AUS920030791US1
Aguilar, et al.
System and Meth d f r Pr c ss r D dicat d Code Handling in a Multi-Proc ss r Environm nt
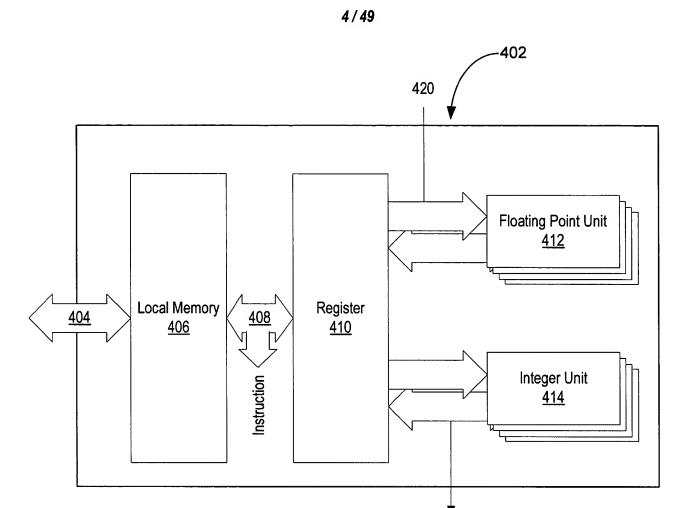
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Figure 7

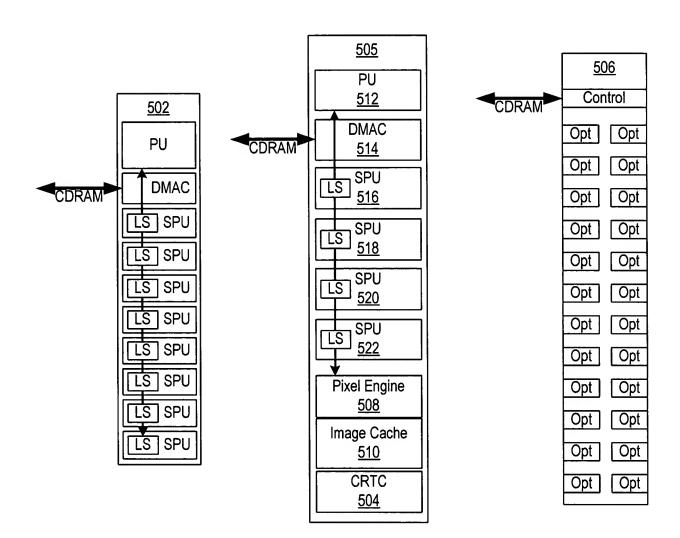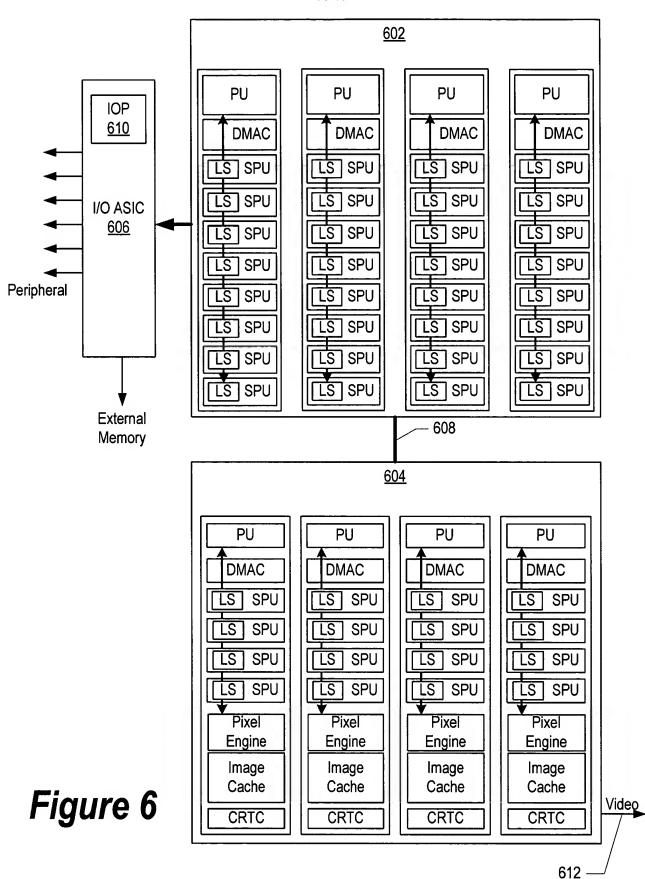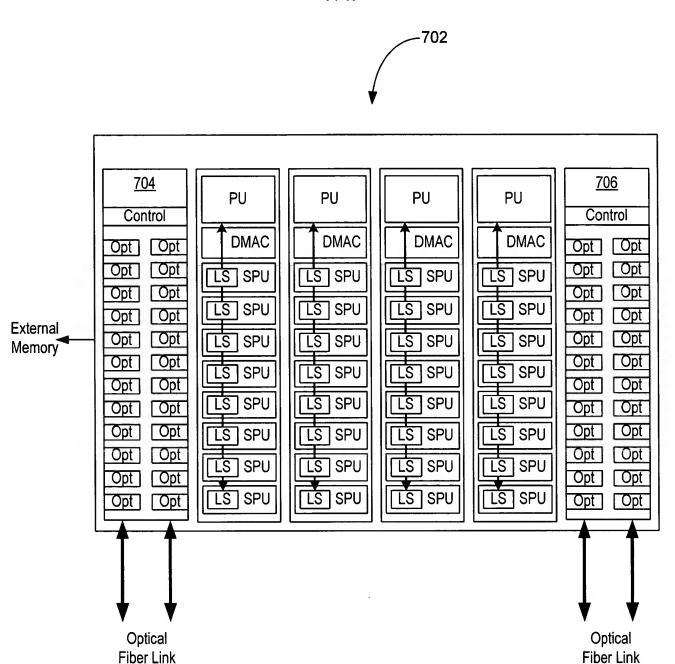Fil : 3050.VSD   Docket No. AUS920030791US1
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Figure 8

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```
                                    ┌──────────────────────────────┐
                                    │  ┌───────────┐  ┌───────────┐ │
                                    │  │    902    │  │    904    │ │
                                    │  │ ┌───────┐ │  │ ┌───────┐ │ │
                                    │  │ │  PE   │ │  │ │  PU   │ │ │
                                    │  │ └───────┘ │  │ └───────┘ │ │
                                    │  │ ┌───────┐ │  │ ┌───────┐ │ │
                                    │  │ │ DMAC  │ │  │ │ DMAC  │ │ │
                                    │  │ └───────┘ │  │ └───────┘ │ │
         ┌─────────────┐           │  │ ┌──┬────┐ │  │ ┌──┬────┐ │ │
◄────    │             │           │  │ │LS│SPU │ │  │ │LS│SPU │ │ │
◄────    │             │           │  │ └──┴────┘ │  │ └──┴────┘ │ │
◄────    │  I/O ASIC   │           │  │ ┌──┬────┐ │  │ ┌──┬────┐ │ │
◄────    │    906      │───────────│  │ │LS│SPU │ │  │ │LS│SPU │ │ │
◄────    │             │           │  │ └──┴────┘ │  │ └──┴────┘ │ │
◄────    │             │           │  │ ┌──┬────┐ │  │ ┌──┬────┐ │ │
         └─────────────┘           │  │ │LS│SPU │ │  │ │LS│SPU │ │ │
Peripheral                         │  │ └──┴────┘ │  │ └──┴────┘ │ │
```

Peripheral

I/O ASIC 906

External Memory

902: PE, DMAC, LS SPU, LS SPU, LS SPU, LS SPU, LS SPU, LS SPU, LS SPU, LS SPU

904: PU, DMAC, LS SPU, LS SPU, LS SPU, LS SPU, Pixel Engine, Image Cache, CRTC

Video

Figure 9

File: 3050.VSD

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Figure 10

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1126

1130

1118

1102

1122

1104 Optical I/O

PE 1110

PE 1112

PE 1114

PE 1116

Optical I/O 1106

1120

1108

1124

1128

1132

Figure 11A

1152

1154

1156

1166

1160

1162

1164

Figure 11B

1176

1172

1182

1178

1174

1188

1184

1180

1190

1186

Figure 11C

Figure 12A

Figure 12B
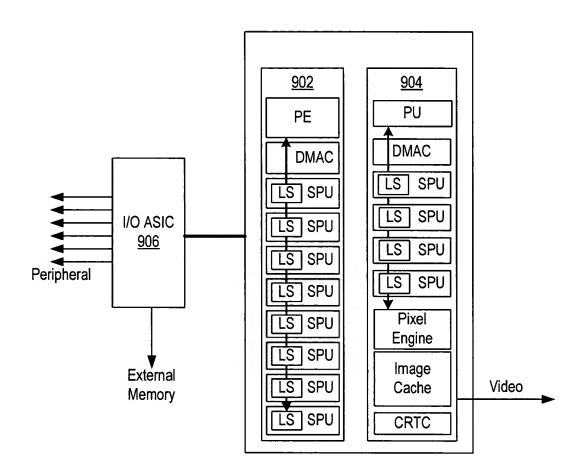
File: 3050.VSD   Docket No. AUS920030791US1
                              Aguilar, et al.
        Syst m and M thod f r Pr c ss r Dedicated Cod Handling in a Multi-Proc ss r Envir nment

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Figure 13

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Figure 14A

Figure 14B

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Figure 15

Fil : 3050.VSD   D cket N . AUS920030791US1
Aguilar, t al.
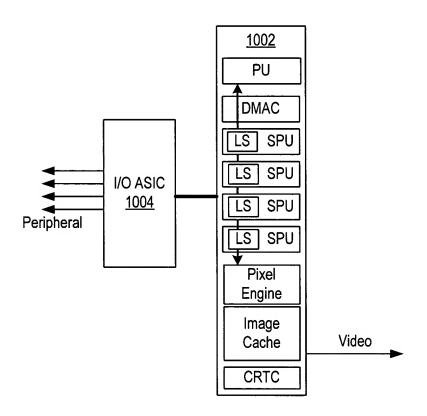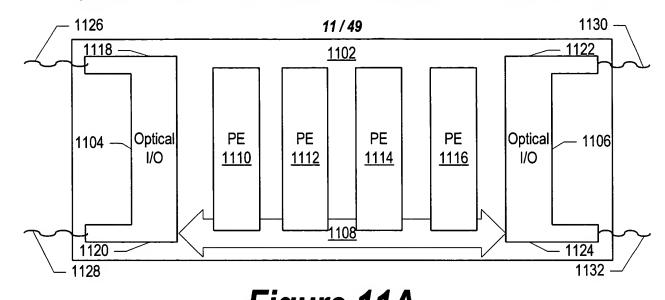Syst m and Method for Pr cessor Dedicated C de Handling in a Multi-Pr cessor Envir nm nt

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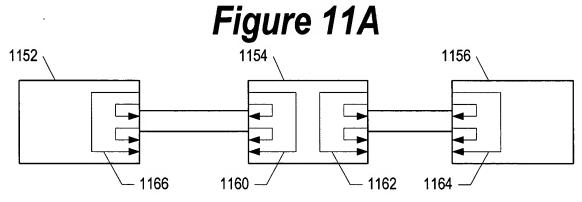
```
                ┌──────────┐
                │   PU     │
                │  1604    │
                └──────────┘

                ┌──────────┐                              ┌─────────────────────┐
                │  DMAC    │         1608                 │                     │
        ──────→ │  1606    │  ═══════════════════════⟹   │       DRAM          │
                └──────────┘                              │       1610          │
                                                          │                     │
1607 ───                                                  │                     │
                ┌──────────┐                              │                     │
                │  SPU     │                              └─────────────────────┘
        ──────→ │  1602    │
                └──────────┘


                ┌──────────┐
                │  SPU     │
                │  1602    │
                └──────────┘

                     0
                     0
                     0
```

Figure 16

File: 3050.VSD   Docket No. AUS920030791US1
Aguilar, t al.
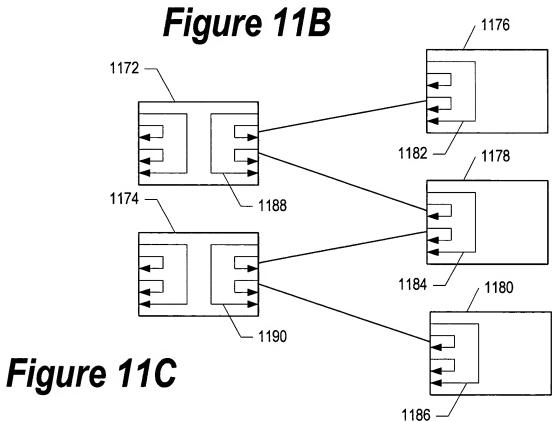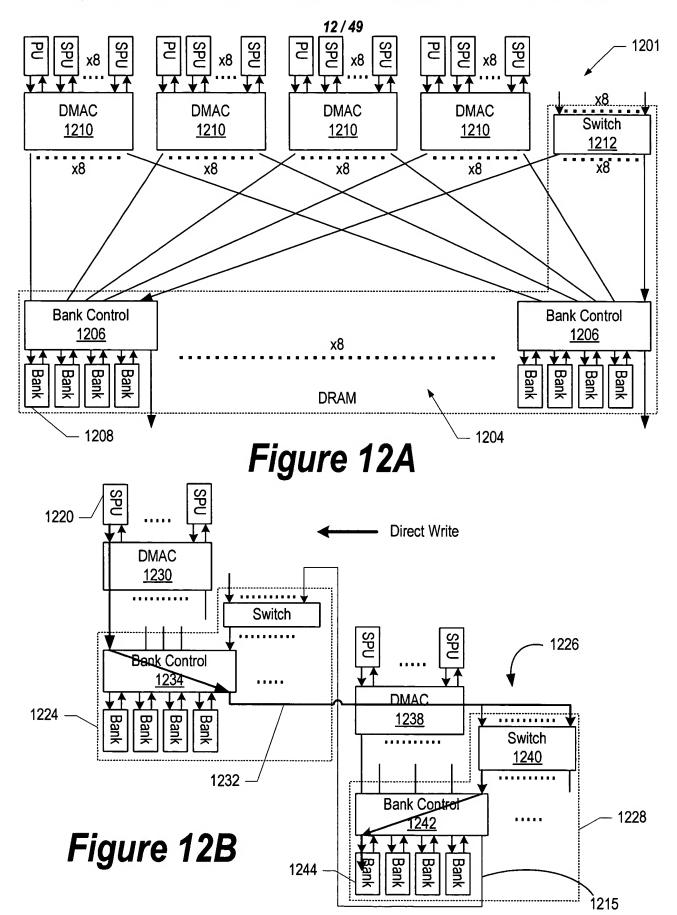System and Method for Processor Dedicated Cod Handling in a Multi-Pr cess r Environment

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Figure 17

File: 3050.VSD

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Aguilar, et al.
System and Method for Processor Dedicated Code Handling in a Multi-Processor Environment

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Figure 18

File: 3050.VSD

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Aguilar, et al.
System and Method for Processor Dedicated Code Handling in a Multi-Processor Environment

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Figure 19

File: 3050.VSD   Docket No. AUS920030791US1
Aguilar, et al.
Syst m and Method for Pr cess r Dedicat d Code Handling in a Multi-Pr c ss r Envir nment

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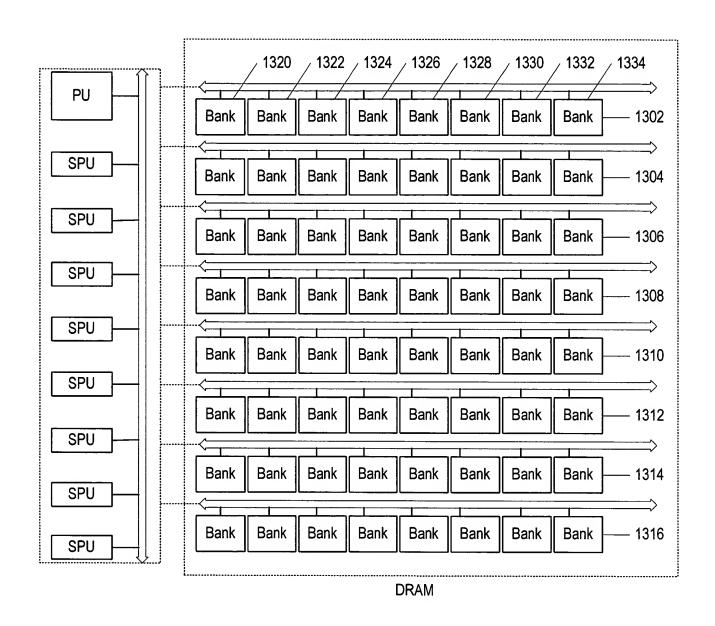**Figure 20**

Figure 21

Fil : 3050.VSD   Docket No. AUS920030791US1
Aguilar, et al.
System and Method for Process r Dedicated Cod Handling in a Multi-Pr c ss r Envir nm nt

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Control

B   Data

Local Storage

SPU

Control

B   Data

1

Local Storage

SPU

1750

1752

1740

PE   1712

F/E	SPU ID	LS Address
0		

Data

Status

X X X

DRAM Bank

1708

1702

Figure 22

Figure 23

File: 3050.VSD

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Aguilar, et al.
System and Meth d f r Proc ss r Dedicated Cod Handling in a Multi-Proc ss r Envir nm nt

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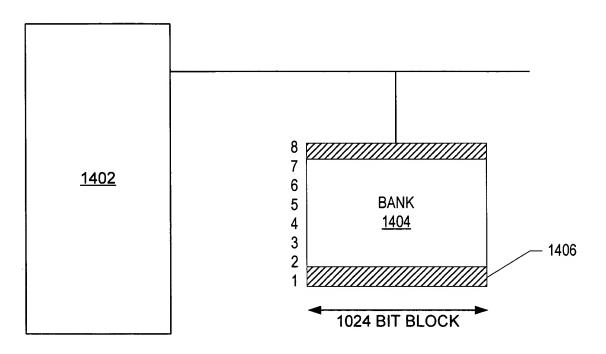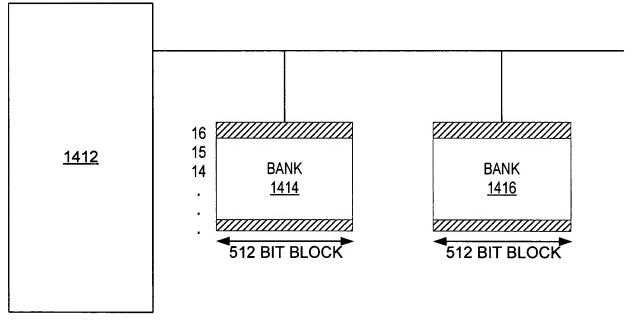**Figure 24**

Figure 25

Fil : 3050.VSD

System and Method for Processor Dedicated Code Handling in a Multi-Processor Environment
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Figure 26

Figure 27

Figure 28

File: 3050.VSD

Dock t No. AUS920030791US1
Aguilar, et al.
System and Method for Processor Dedicated Code Handling in a Multi-Processor Environment
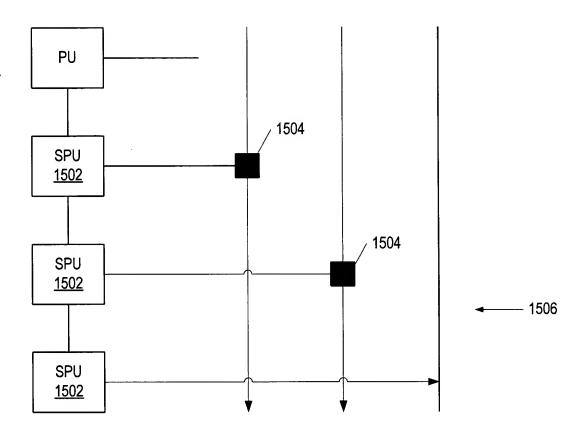
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Figure 29

File: 3050.VSD

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System and Method for Processor Dedicated Code Handling in a Multi-Processor Environment

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Figure 30

Figure 31

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Aguilar, et al.
System and M thod f r Pr cessor Dedicated Code Handling in a Multi-Proc ss r Envir nm nt

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Sync. Write Error

Full
3282

Sync. Read

Sync. Write

Sync. Read Error

Empty
3280

Sync. Write

Blocking
3284

Sync. Read

Figure 32

File: 3050.VSD   Docket No. AUS920030791US1
Aguilar, et al.
Syst m and Method f r Pr c ss r Dedicated Code Handling in a Multi-Pr c ssor Envir nment

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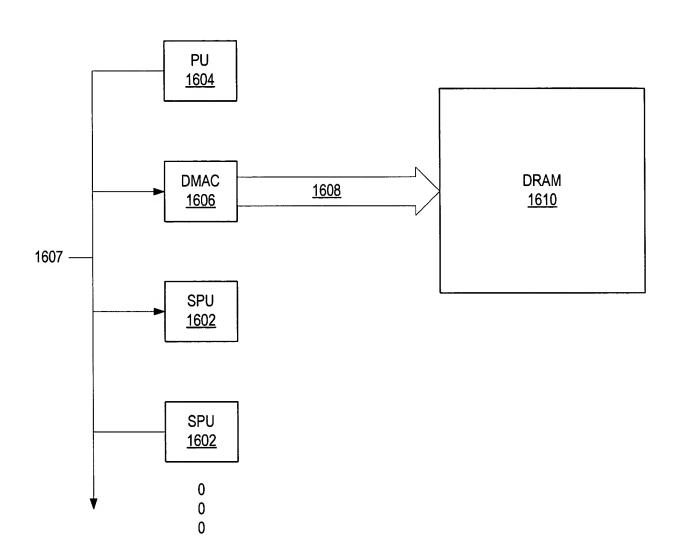Key Control Table

3302

3304   3306   3308

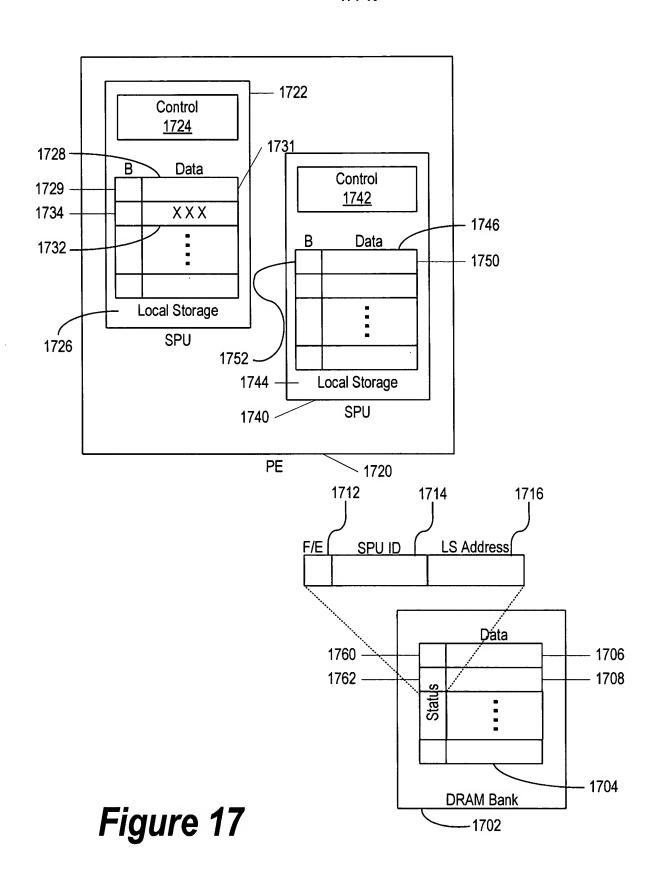| ID		
o	SPU Key	Key Mask
1	SPU Key	Key Mask
2	SPU Key	Key Mask
	⋮	
7	SPU Key	Key Mask

Figure 33

Fil : 3050.VSD   Docket No. AUS920030791US1
Aguilar, t al.
Syst m and M th d for Processor Dedicated Code Handling in a Multi-Pr c ss r Environm nt

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DATA	SYNCH INFO	KEY
	. . . . . .	

3406

3408

3410

3412

3402

Figure 34

File: 3050.VSD   Docket No. AUS920030791US1
                              Aguilar, t al.
      System and M thod f r Proc ssor Dedicated C de Handling in a Multi-Pr c ss r Environm nt
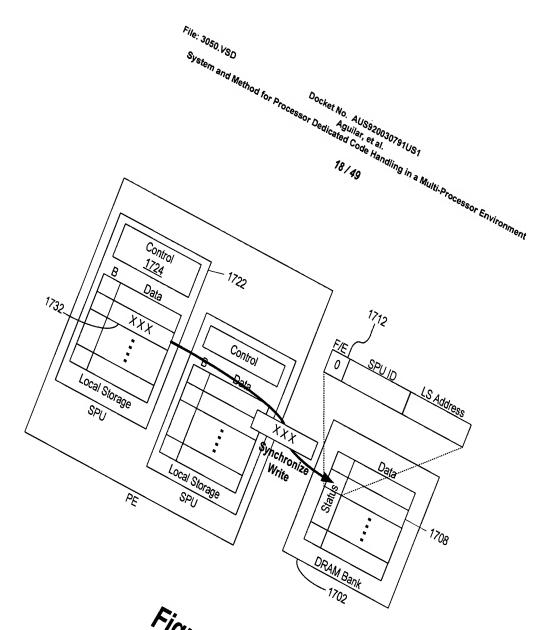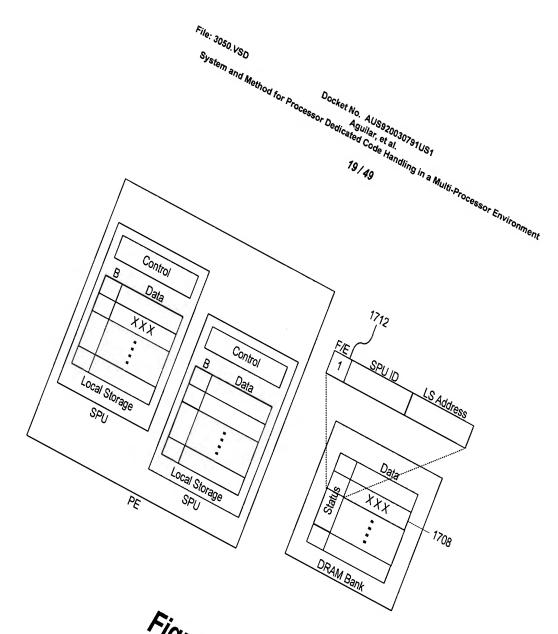
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Memory Access Control Table

ID	Base	Size	Access Key	Access Key Mask
o	Base	Size	Access Key	Access Key Mask
1	Base	Size	Access Key	Access Key Mask
2	Base	Size	Access Key	Access Key Mask
		⋮		
63	Base	Size	Access Key	Access Key Mask

3504 3506 3508 3510 3512 3502

Figure 35

Fil : 3050.VSD

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System and Meth d for Process r Dedicated Code Handling in a Multi-Pr cess r Environment

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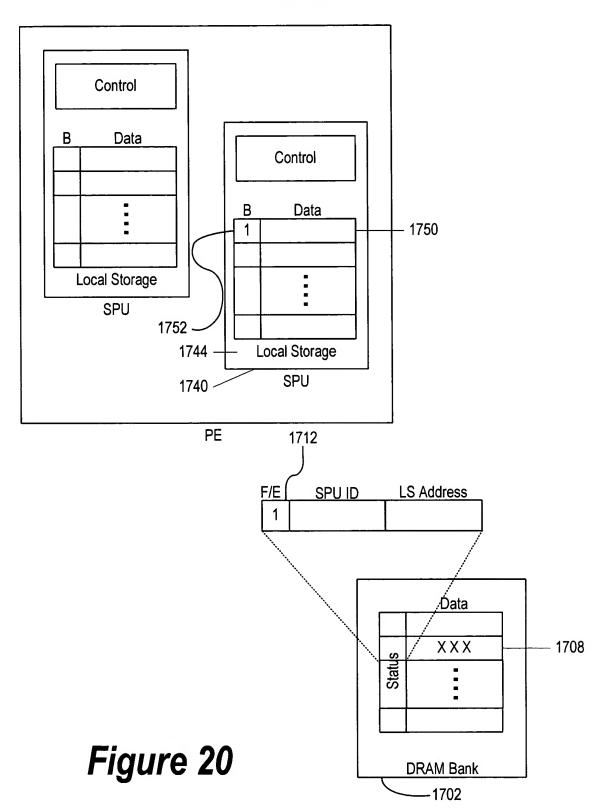SPU Issues DMA Command
3602

DMAC Looks Up SPU's Key
3604

DMAC Looks Up Memory
Access Key
3606

DMAC Compares SPU Key to
Access Key
3608

Match?
3610

No → Error Signal Generated and
Access Prevented
3612

Yes

DMAC Executes DMA
Command
3614

Figure 36

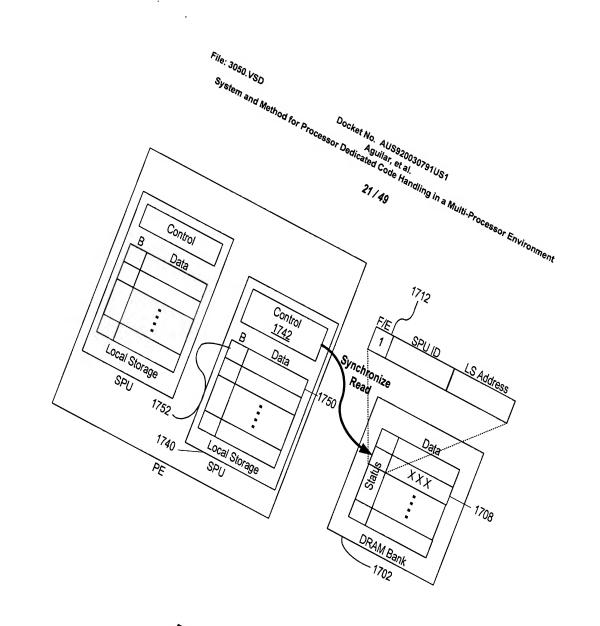Fil : 3050.VSD   Docket No. AUS920030791US1
Aguilar, et al.
System and Meth d f r Process r Dedicat d C de Handling in a Multi-Pr c ss r Envir nm nt

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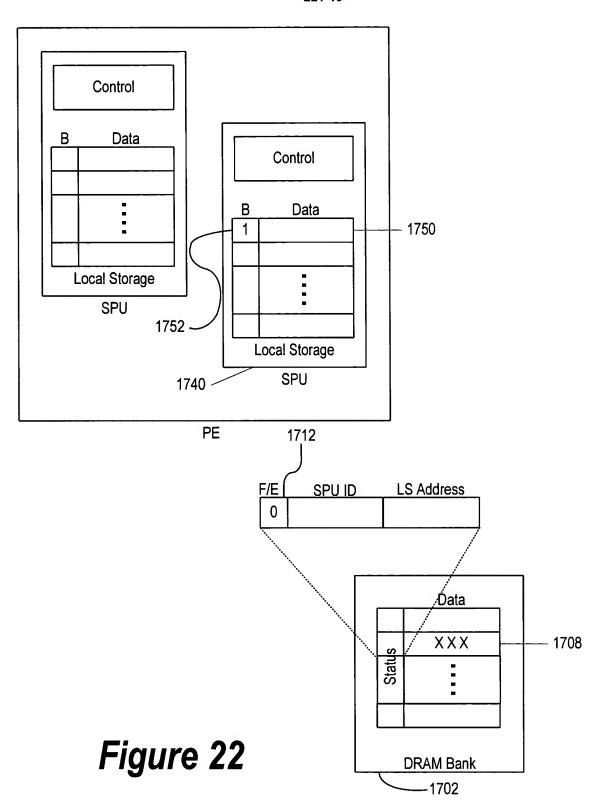
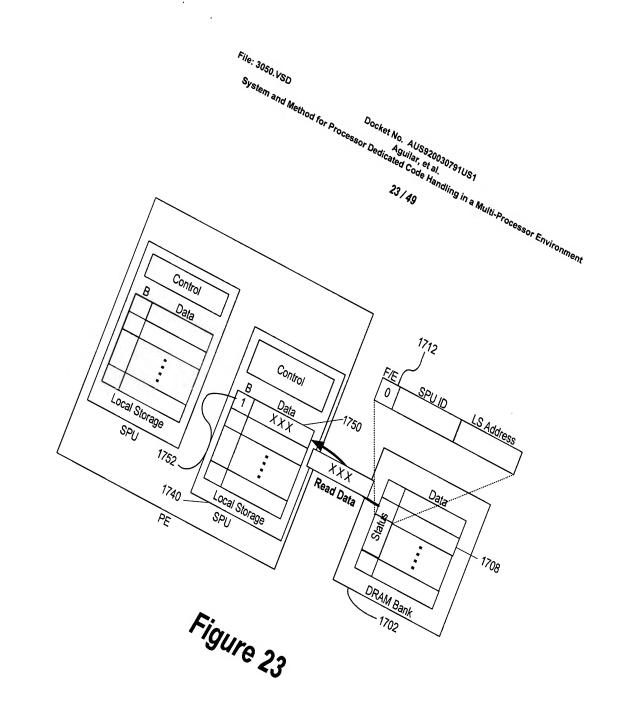| Header 3708 |
|---|
| Destination ID 3710 |
| Source ID 3712 |
| Reply ID 3714 |

3704

Header
DMA Commands
SPU Programs
Data

3706

Header 3720
Global Unique ID 3724
Num. of req. SPUs 3726
Sandbox Size 3728
ID of Previous CELL 3730

3722

3740
3742 3744 3746 3748
3750

VID	Load	Addr	LSaddr
VID	Load	Addr	LSaddr

3734

3755
3752 3754 3756
3758

VID	Kick	PC
VID	Kick	PC

3732

SPU Program 3760
SPU Program 3762

3736

Data

3738

3702

Figure 37

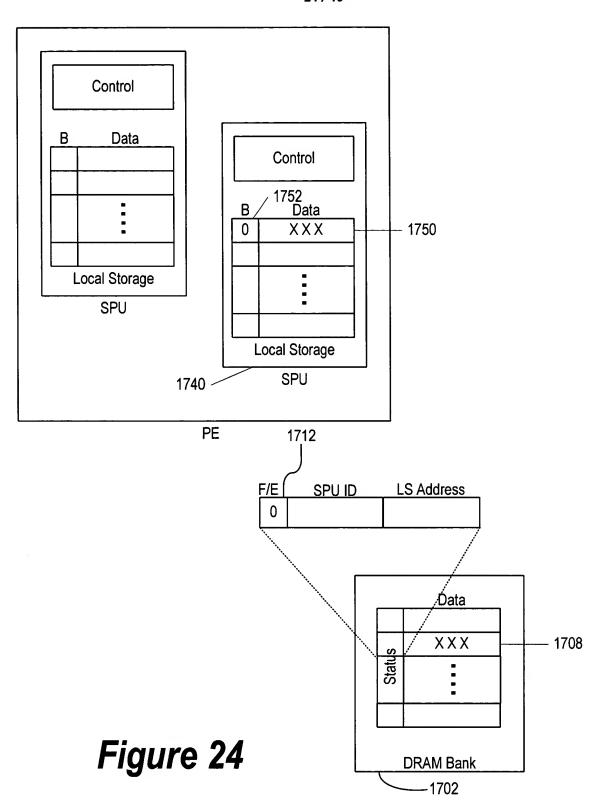Fil : 3050.VSD   Dock t N . AUS920030791US1
Aguilar, et al.
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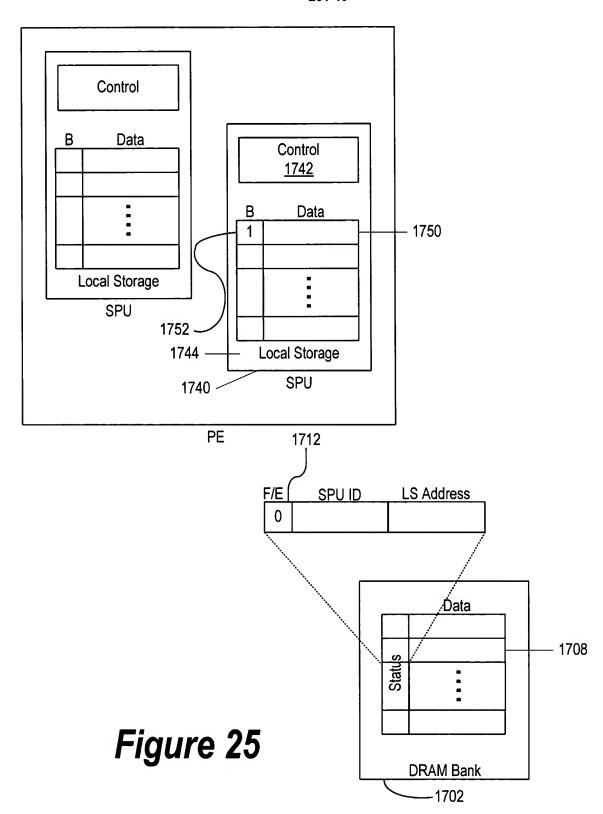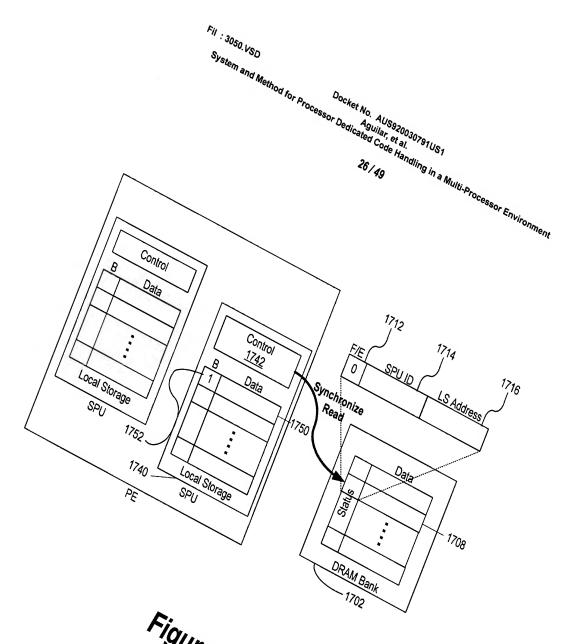
```
┌──────────────┐     ┌──────────────┐     ┌──────────────┐     ┌──────────────┐
│ Evaluation and│     │              │     │ PU Enables an│     │  PU Issues   │
│Designation of │     │ PU Allocates │     │  Interrupt   │     │     DMA      │
│    SPUs       │ ──► │ DRAM Memory  │ ──► │Request for the│ ──►│ Command to   │         3802
│              │     │    3812      │     │     SPU      │     │ Load Spulet  │
│    3810       │     │              │     │    3814      │     │    3818      │
└──────────────┘     └──────────────┘     └──────────────┘     └──────────────┘
```

```
┌────────┐   ┌──────────┐   ┌────────┐   ┌──────────┐   ┌──────────┐   ┌──────────┐
│Spulet Read│ │PU Issues DMA│ │ Stack  │  │PU Issues DMA│ │DMAC Updates│ │PU Issues DMA│
│from DRAM  │ │Command to  │ │ Frame  │  │Command to  │ │Key Control │ │Command Kick│
│to Local   │►│Load Stack  │►│Read from│►│Assign Key  │►│  Table     │►│to Start Spulet│
│Storage    │ │Frame       │ │DRAM to │  │   3824     │ │  3826      │ │   3828     │
│  3820     │ │  3822      │ │ Local  │  │            │ │            │ │            │
└────────┘   └──────────┘   │Storage │  └──────────┘   └──────────┘   └──────────┘
                            │  3823  │
                            └────────┘
```

```
         ┌──────────────┐   ┌──────────────┐   ┌──────────────┐   ┌──────────┐
         │ SPU Begins   │   │              │   │  SPU Issues  │   │ Data Read│
         │ Execution of │   │SPU Evaluates │   │ Multiple DMA │   │  from    │
  3804   │   Spulet     │──►│ Stack Frame  │──►│ Commands to  │──►│ DRAM to  │
         │    3830      │   │    3832      │   │ Load Data in │   │  Local   │
         │              │   │              │   │Local Storage │   │ Storage  │
         └──────────────┘   └──────────────┘   │    3834      │   │  3836    │
                                               └──────────────┘   └──────────┘
```

```
         ┌──────────────┐   ┌──────────────┐   ┌──────────┐   ┌──────────────┐
         │   Spulet     │   │  SPU Issues  │   │  Result  │   │              │
         │  Processes   │   │     DMA       │   │ Written  │   │  SPU Issues  │
         │  Spulet and  │──►│ Command to   │──►│from Local│──►│  Interupt    │
         │  Provides    │   │Store Reslut in│  │Storage to│   │ Request to PU│
         │   Reslut     │   │    DRAM      │   │  DRAM    │   │    3844      │
         │    3838      │   │    3840      │   │  3842    │   │              │
         └──────────────┘   └──────────────┘   └──────────┘   └──────────────┘
```

Figure 38

Figure 39

Fil : 3050.VSD   Docket No. AUS920030791US1
                              Aguilar, et al.
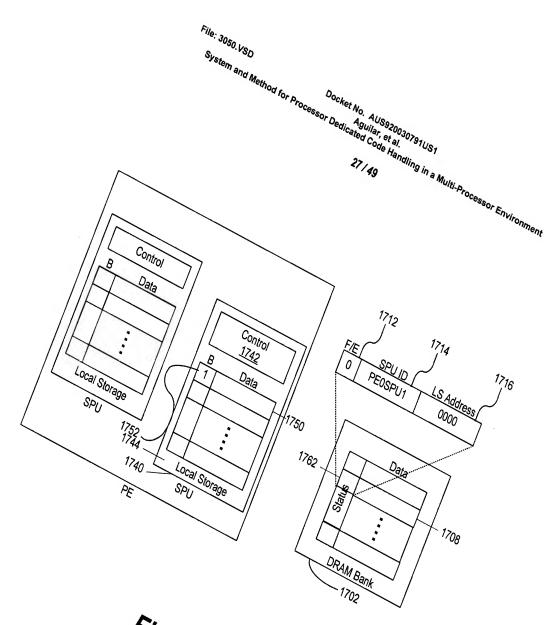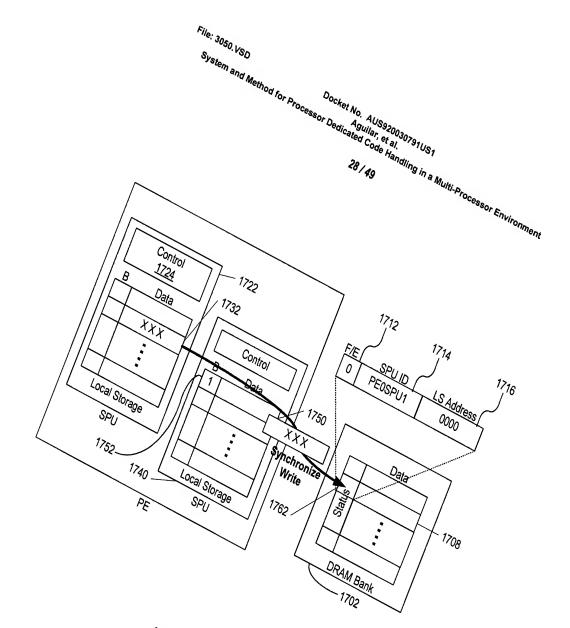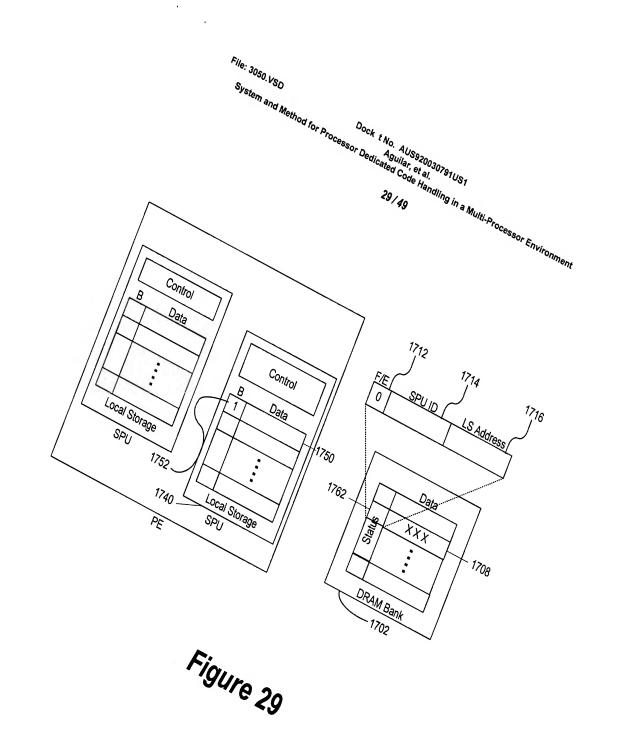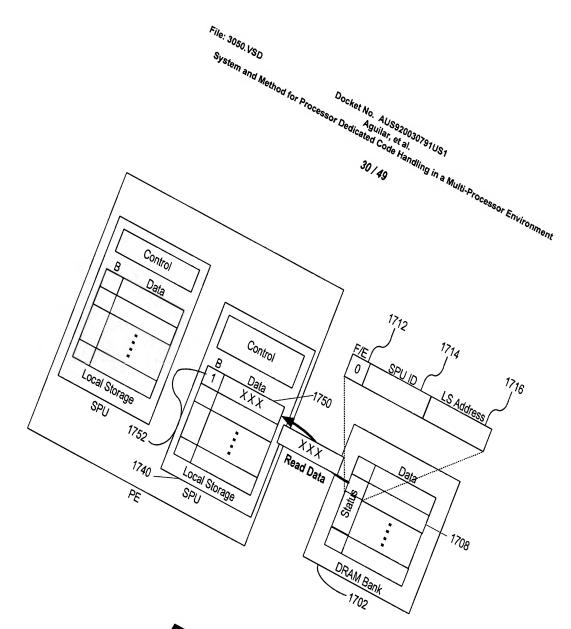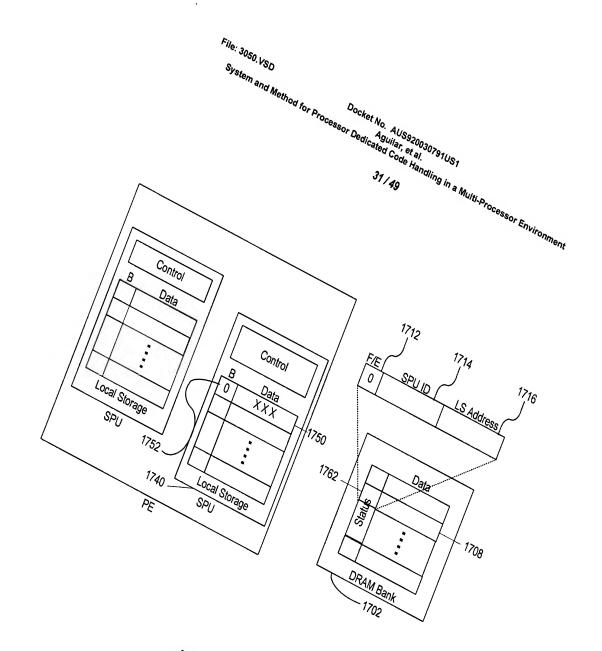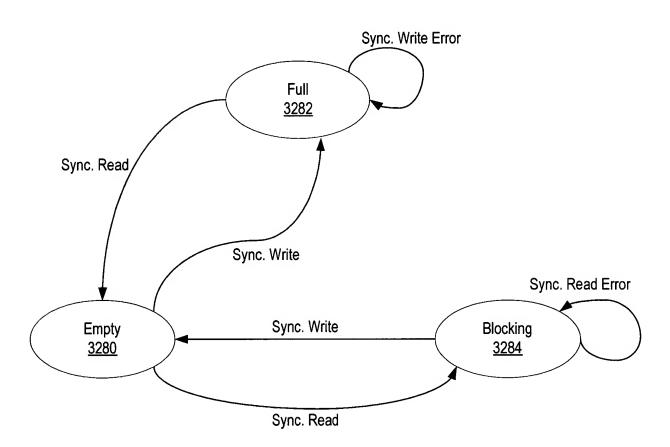   System and Meth d f r Proc ssor D dicated Code Handling in a Multi-Pr c ss r Environment

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| PU Assigns SPU to Process Network Spulet 4010 | PU Instructs SPU to Perform Resident Terminations 4012 | PU Assigns SPUs to Process MPEG Applets 4014 | PU Instructs SPUs to Perform Resident Terminations 4015 | PU Designates a Source Memory Sandbox 4016 | PU Designtes a Destination Memory Sandbox 4018 |

| PU Designates a Source Memory Sandbox 4020 | PU Designates a Destination Memory Sandbox 4022 | Decoding SPU Sets up Source Sandboxes with Synchronize Read Commands 4024 | Establishment of Dedicated Pipeline Complete 4028 |

Figure 40A

| Network SPU Receives TCP/IP Packets 4030 | TCP/IP Packets Assembled into Software Cell by Network SPU 4032 | Type of Software Cell Determined 4034 | MPEG Data Cell → Previous Cell ID Read by Network SPU 4038 | Network SPU Chooses a Decoding SPU in the Pipeline for Processing MPEG DATA 4040 |

Other

Transmit to General Purpose Sandbox 4036

| MPEG Data Synchronize Written from Network SPU to Source Sandbox 4042 | MPEG Data Automatically Read from Source Sandbox to Decoding SPU 4044 | Decoding SPU Decodes MPEG Data into Video Data 4046 | Decoding SPU Writes Video Data to Destination Sandbox 4048 | Decoding SPU Sets up Source Sandbox with Synchronize Read Command 4050 | Decoding SPU Placed is Resident Termination 4052 |

Figure 40B

File: 3050.VSD   Docket No. AUS920030791US1
                        Aguilar, et al.
Syst m and Method for Pr c ssor Dedicated Code Handling in a Multi-Pr cess r Envir nm nt
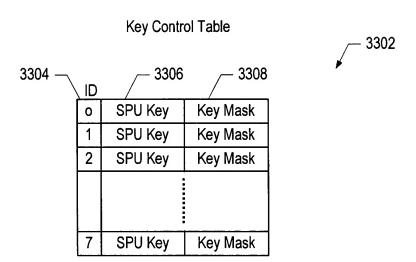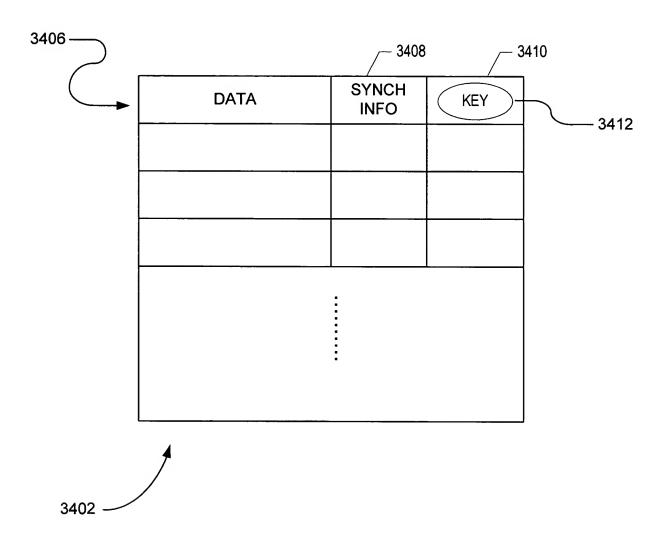
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Figure 41

File: 3050.VSD   D cket No. AUS920030791US1
                              Aguilar, et al.
Syst m and M th d f r Pr c ss r Dedicat d Code Handling in a Multi-Pr cessor Envir nm nt

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Figure 42

Fil : 3050.VSD   Docket No. AUS920030791US1
                                         Aguilar, et al.
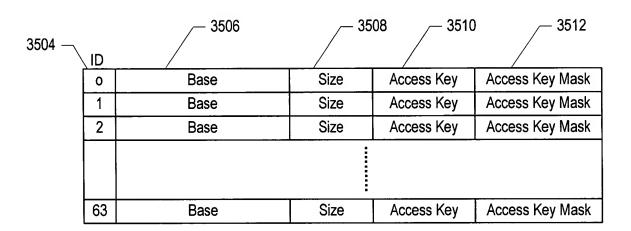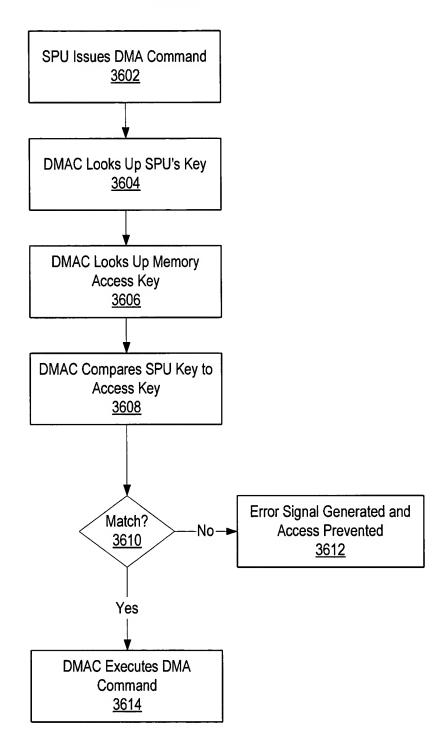   System and Method f r Proc ssor D dicated C de Handling in a Multi-Pr c ssor Environment

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VM Programs (e.g., Java) 4305

Programs Compiled for VM Environment 4300

VM Engine (e.g., JVM) 4315

Virtual Machine Software (Run on an SPU) 4310

Processor, Hardware Platform, Operation System 4320

PE 4330

SPU (Running VM) 4340

Other SPUs 4335

Processor Element 4325

Figure 43A

4350

PU / SPU

Programs Compiled for VM Environment 4360

Instructions Executable by Processor (PU or SPU) 4380

DMA

DMA

4370

SPU

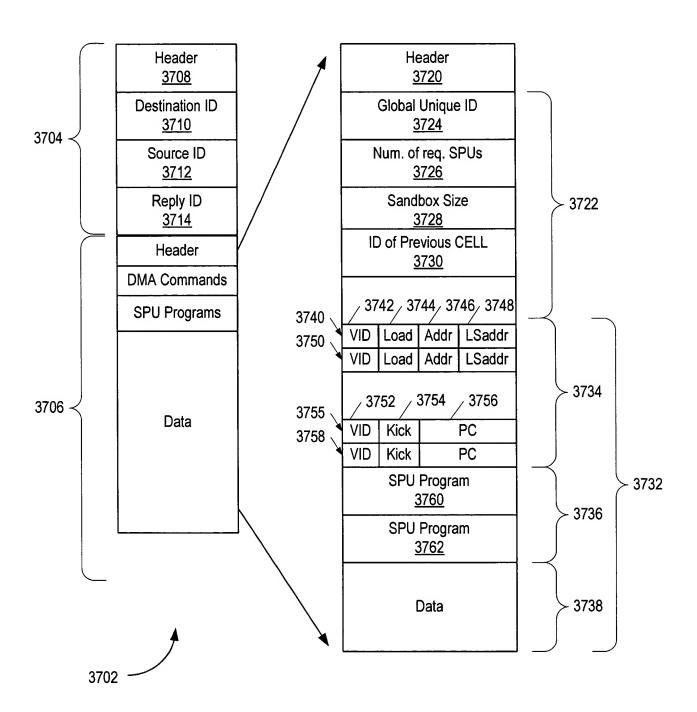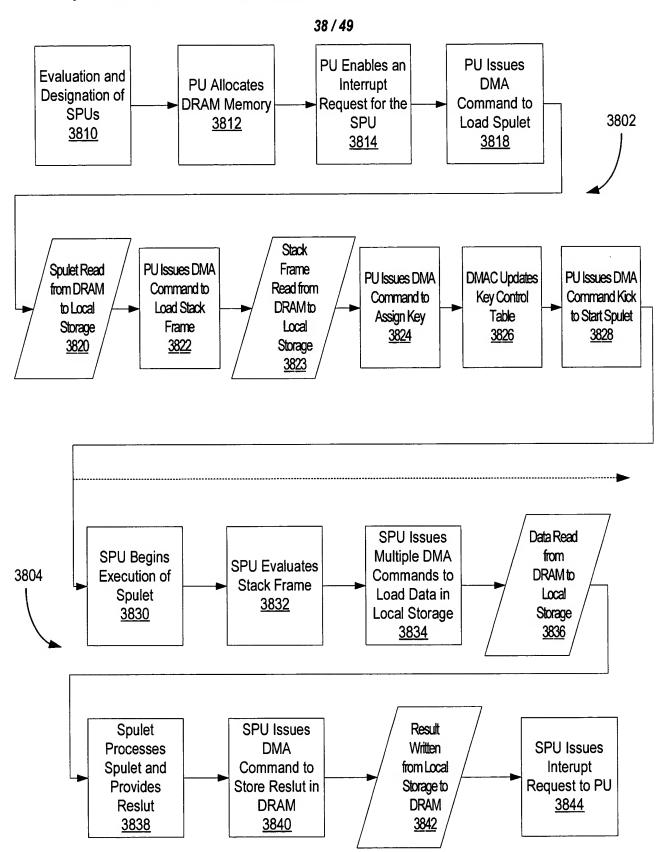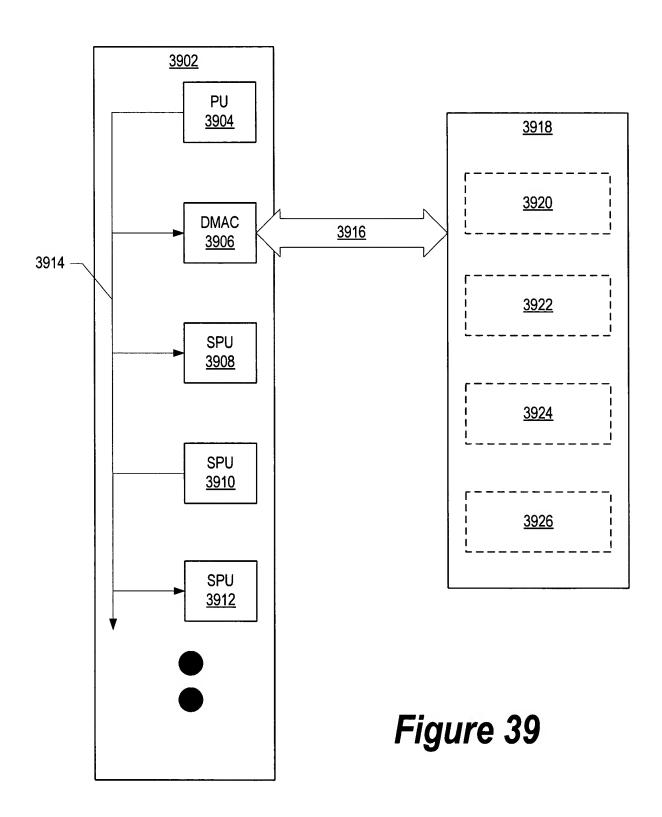**Virtual Machine Software (Loaded Upon Initialization or When Needed)**

Figure 43B

Fil : 3050.VSD

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System and Method f r Pr c ss r D dicat d Code Handling in a Multi-Pr cess r Environment

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4425

PU Environment
4400

SPU Mailbox

| Request 1 |
| Request 2 |
| Request 3 |
| ⋮ |

SPU
4430

↓

Load VM Code
4405

Receive Request
4435

↓

Request SPU to Interpret VM Code
4415

4410

Retrieve VM Code Identified in Request
4440

Common Memory Map

DMA

Process Waits for Interpreted Code. PU Free to Perform other tasks while waiting.
4420

| VM Code 4412 |
| |

Process VM Code Using SPU-Based Virtual Machine Program Resulting in Instructions Suitable for Requesting Process' Operating Environment (PU or SPU)
4445

| Executable Instructions 4414 |
| |

DMA

Execute (Jump to) Instructions Prepared by SPU
4480

Write Instructions to Common Memory
4450

↓

Signal Requesting Process that Code Ready
4455

End
4490

End
4460

Figure 44

PU Gaming Environment
4500

Execute Main Line Video Game Application
4505

Upcoming Effect Needed?
4510

4518 — No

4512 — Yes

Request Effect
4515

4520

SPU Mailbox

Request 1

Request 2

Request 3

⋮

SPU Effect Engine
4525

Receive Request and Parameters
4530

Effect Code in Local Storage?
4535

4538 — No

4542 — Yes

Retrieve Effect Code from Common Memory
4540

DMA

4550

Common Memory

Effect Code
4555

Executable Effect
4560

Launch Effect?
4580

No

4582

4584

Yes

Execute Instructions Prepared by SPU to Provide Effect
4585

Process Effect Code Using SPU-Based Program Resulting in PU-Instructions to Perform Effect
4545

4592

No

End?
4590

4594 — Yes

Write PU Instructions to Common Memory
4565

Signal PU Application that Effect Ready
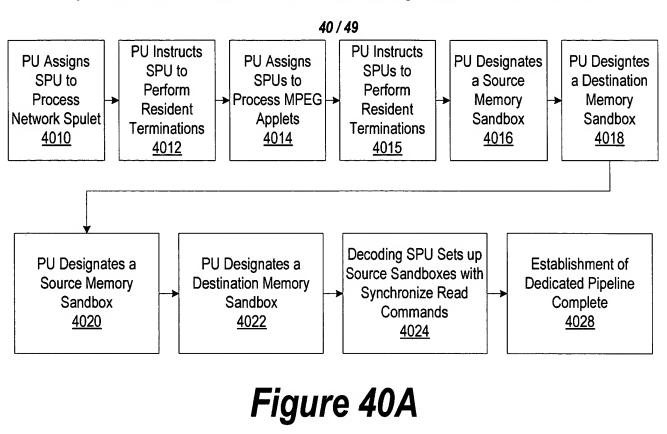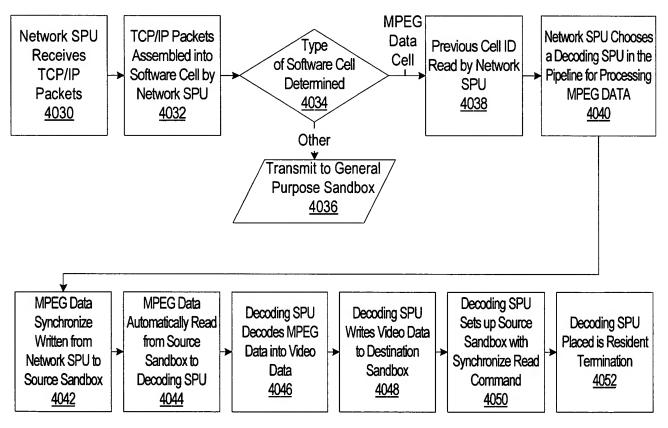4570

End
4595

End
4575

Figure 45

File: 3050.VSD   D cket No. AUS920030791US1
Aguilar, et al.
System and Meth d f r Pr c ssor Dedicated Code Handling in a Multi-Pr cessor Envir nment

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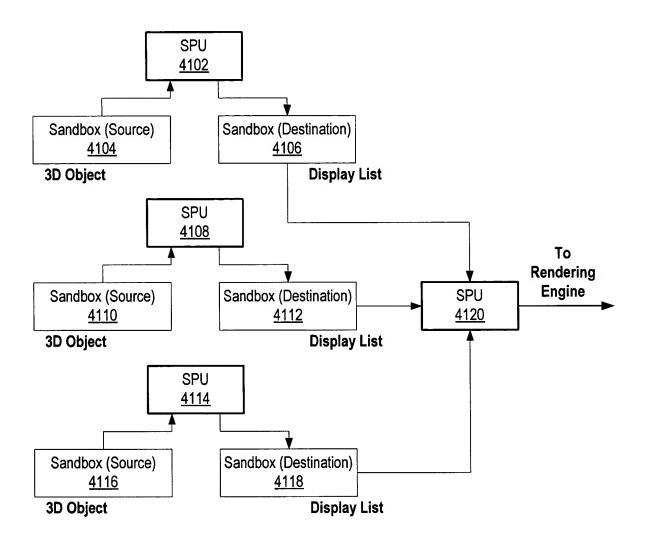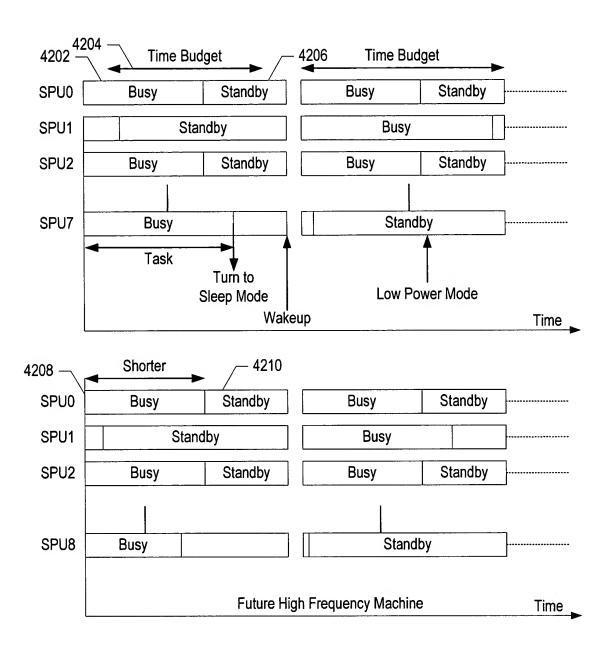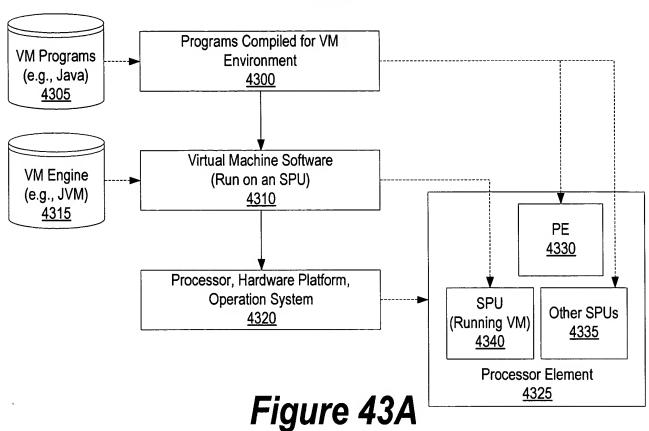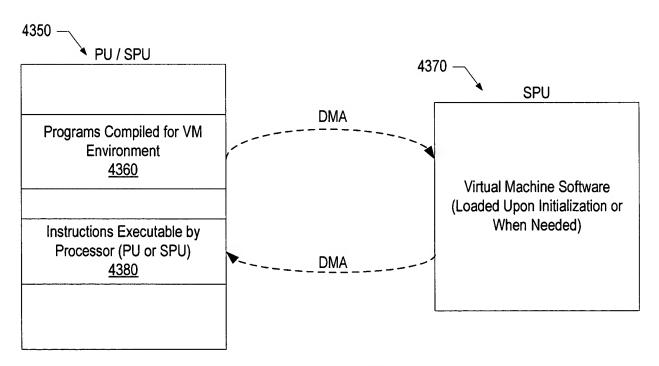
```
                    ┌─────────────────────────┐
                    │  Game Program Example   │
                    │          4600           │
                    └────────────┬────────────┘
                                 │
                    ┌────────────▼────────────┐
                    │         START           │
                    │          4605           │
                    └────────────┬────────────┘
                                 │
        4612                ┌────▼────┐                4648
                  "Jungle"  │  User   │  "Warehouse"
              ┌─────────────│ Selects │──────────────┐
              │             │  Path   │              │
              │             │  4610   │              │
              │             └─────────┘              │
    ┌─────────▼──────────┐            ┌──────────────▼─────┐
    │ Request Lion Roar  │            │ Request Explosion  │
    │  Effect from SPU   │            │  Effect from SPU   │
    │       4615         │            │       4650         │
    └─────────┬──────────┘            └──────────────┬─────┘
    ┌─────────▼──────────┐            ┌──────────────▼─────┐
    │ Request Bear Growl │            │ Request Monster    │
    │  Effect from SPU   │            │  Effect from SPU   │
    │       4620         │            │       4655         │
    └─────────┬──────────┘            └──────────────┬─────┘
    ┌─────────▼──────────┐            ┌──────────────▼─────┐
    │ User's Character   │            │ User's Character   │
    │    Movement        │            │    Movement        │
    │       4625         │            │       4660         │
    └─────────┬──────────┘            └──────────────┬─────┘
  4632             ┌──────▼──────┐       4668         ┌───────▼──────┐
              Yes  │  Close to   │                Yes │    Hits      │
         ┌─────────│ Hidden Lion?│             ┌──────│ Hidden Trip  │
         │         │    4630     │             │      │    Wire?     │
         │         └──────┬──────┘             │      │    4665      │
    ┌────▼────┐        No │               ┌────▼────┐   └──────┬──────┘
    │ Run Lion│           │               │  Run    │       No │
    │  Roar   │───►       │               │Explosion│────►     │
    │ Effect  │           │               │ Effect  │          │
    │  Code   │           │               │  Code   │          │
    │  4635   │           │               │  4670   │          │
    └─────────┘           │               └─────────┘          │
  4642           ┌────────▼────┐      4678         ┌───────────▼──────┐
              Yes│  Close to   │                Yes│   Walks into     │
         ┌───────│Hidden Bear? │             ┌─────│ Storage Room?    │
         │       │    4640     │             │     │     4675         │
         │       └──────┬──────┘             │     └───────┬──────────┘
    ┌────▼────┐      No │               ┌────▼────┐      No │
    │Run Bear │         │               │   Run   │         │
    │ Growl   │────►    │               │ Monster │────►    │
    │ Effect  │         │               │ Effect  │         │
    │  Code   │         │               │  Code   │         │
    │  4645   │         ▼               │  4680   │         ▼
    └─────────┘                         └─────────┘
```

Figure 46

Fil : 3050.VSD   Dock t N . AUS920030791US1
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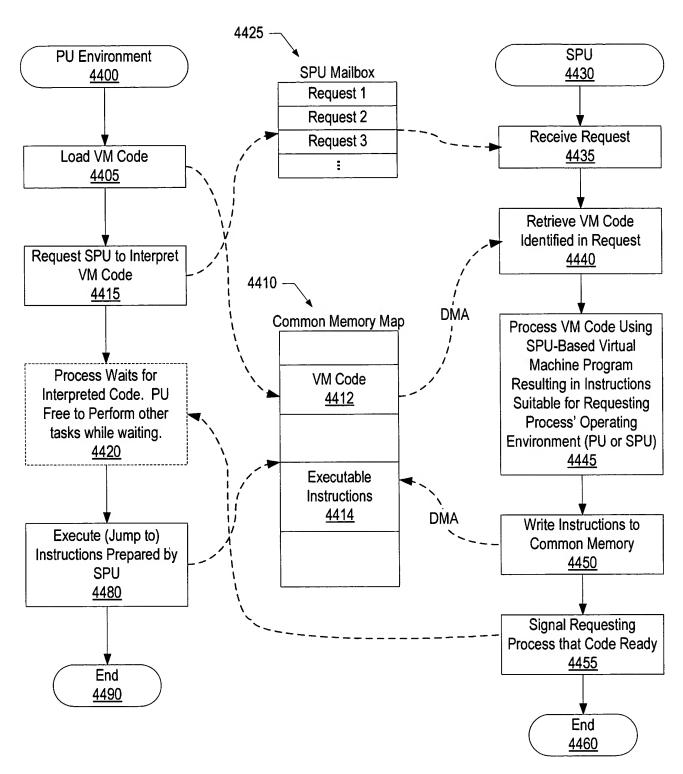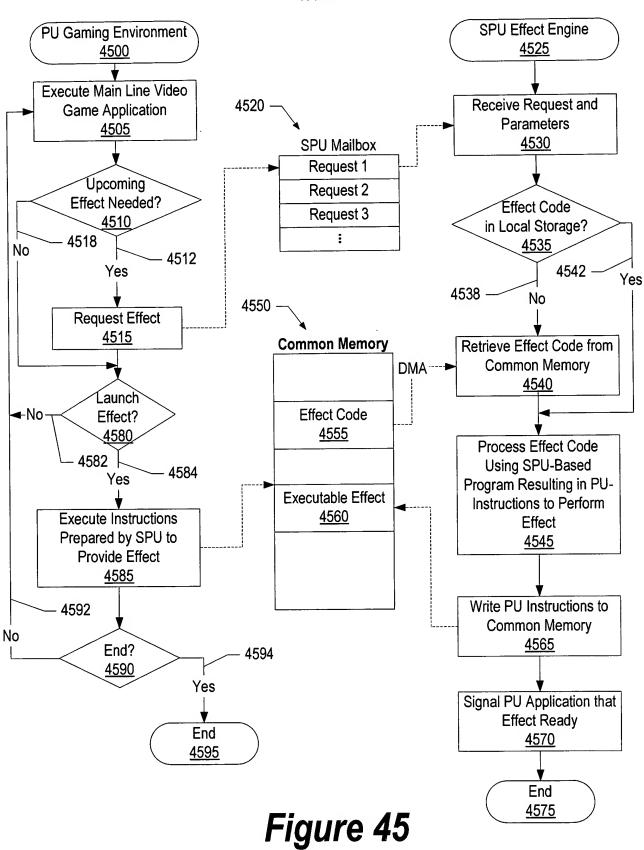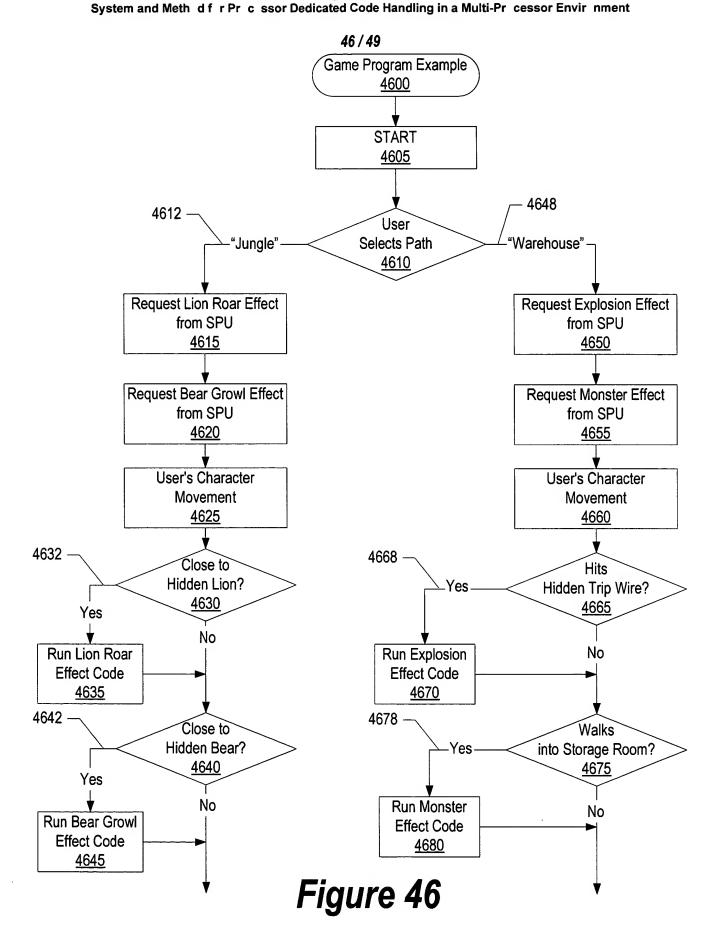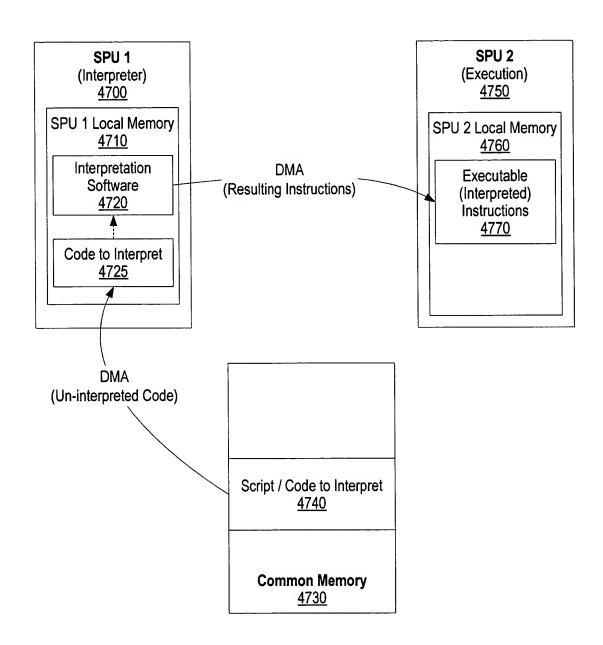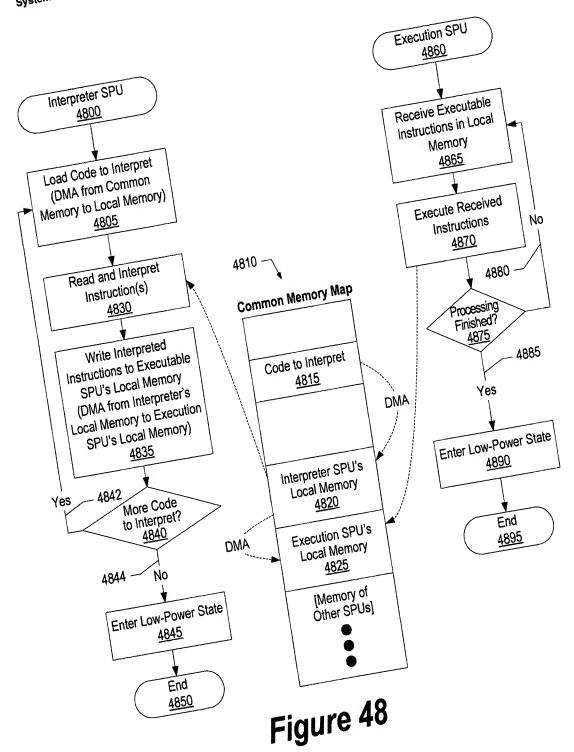*Figure 47*

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Fil : 3050.VSD

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Interpreter SPU
4800

Load Code to Interpret
(DMA from Common
Memory to Local Memory)
4805

Read and Interpret
Instruction(s)
4830

Write Interpreted
Instructions to Executable
SPU's Local Memory
(DMA from Interpreter's
Local Memory to Execution
SPU's Local Memory)
4835

Yes   4842

More Code
to Interpret?
4840

4844   No

Enter Low-Power State
4845

End
4850

4810

Common Memory Map

Code to Interpret
4815

DMA

Interpreter SPU's
Local Memory
4820

DMA

Execution SPU's
Local Memory
4825

[Memory of
Other SPUs]

Execution SPU
4860

Receive Executable
Instructions in Local
Memory
4865

Execute Received
Instructions
4870

No

4880

Processing
Finished?
4875

4885

Yes

Enter Low-Power State
4890

End
4895

Figure 48

File: 3050.VSD   Docket No. AUS920030791US1
Aguilar, et al.
System and Method for Processor Dedicated Code Handling in a Multi-Processor Environment
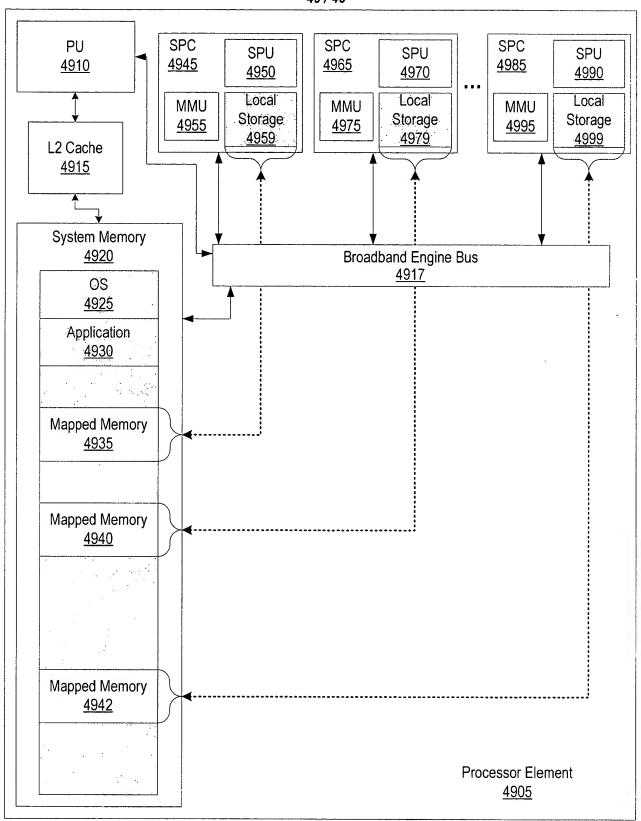
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Figure 49